Specification Amendments

Please amend the specification as follows.

Please amend the paragraphs on page 8, lines 10-14, as follows:

Fig. 6[A] is a diagrammatic sketch of a control processor module and [for the control system architecture of Fig. 5.]

[Fig. 6B is a diagrammatic sketch of] a power supply module for the control system architecture of Fig. 5.

Please amend the paragraph on page 50, line 25, to page 51, line 17, as follows:

The design concept of System Architecture 3 (Fig. 5) is the distribution of control to dedicated, subsystem-specific, microprocessor-based controller modules. Each of these is capable of low-level semi-autonomous control of a particular part of the apparatus mechanism. The controller modules which comprise System Architecture 3 are: a Control Processor 200 for overall control (Fig. 6[A]), one for controlling all aspects of the Carousel Holding Device 262 (Fig. 7A), one for controlling all aspects of the Input Element Station 352 (Fig. 7B), one for controlling all aspects of the Accessing Device Station 394 (Fig. 7C), one for controlling all aspects of the First Fluid Dispensing Station 306 (Fig. 7D), one for controlling all aspects of the Second Fluid Dispensing Station 432 (Fig. 7E), one for controlling all aspects of the Spin Dryer Station 478 (Fig. 7F), and one for controlling all aspects of the Output Element Station 1210 (Fig. 7G). Each controller module performs all of the control (motion, temperature, fluid flow, etc) for a particular station of the present apparatus. Communication among these controller modules occurs by means of a multi-channel shared bus (Fig. 5). The bus originates at, and is supervised by, Control Processor 200. The bus makes the following resources available to every module: isolated 120V AC power (line 212), common system control signals (line 210), IEEE Standard 1149-compatible JTAG scan-bus signals (line 208), intra-apparatus data communications network (line 206), and regulated +24V DC power (line 214). Conditioned power is supplied to each of these modules from a system power supply module 250 (Fig. 6[B]). The actions of each

station controller are governed by embedded real-time executive and application-specific software to control the required tasks and functions. The embedded executive software may be written in processor-specific assembly language or preferably, in C/C++. The custom application-specific software may be written in C/C++.

Please amend the paragraph on page 51, line 19, to page 52, line 13, as follows:

Each of the controller modules of this architecture is described below. The Control Processor 200 (Fig. 6[A]) is based on a 32-bit microprocessor 220, which incorporates non-volatile program storage memory 222 (e.g., based on re-programmable FLASH memory technology) to contain the embedded control software, non-volatile boot-memory 224 to aid in system start-up and initialization, static data RAM 230, and various digital I/O interfaces. Digital I/O interface 228 communicates with front-panel displays and operator controls 216 to permit operators to observe and interact with the apparatus. Interface 234 and sensor 218 support reading of the bar codes associated with each support housing. Digital interface 236 generates the various common system control signals needed by each module of the system. Common system control signals, for example, system clock, reset, interrupts, and the like, are conveyed to the other modules via multi-signal line 210. Digital communication among the modules of the system for the purposes of synchronizing action and communicating process data and status are supported by digital interface 244 via line 206. IEEE Standard 1149-compatible JTAG scan-bus communication among the modules of the system for the purposes of diagnostic testing and fault detection is supervised by scan-bus controller and interface 240 via lines 208. Elements 238 and 242 contain circuitry to support Control Processor self-testing for diagnostic purposes. They include an RS-232 digital I/O interface 204, which serves as a diagnostic port to external test systems. Such systems may be used to control and test the apparatus in ways that are more rigorous than, and differ from, normal operation. Communication with external systems occurs through the 10/100 BaseT Ethernet interface 232 via lines 202. This interface provides 10 Mbps or 100 Mbps serial data communication to supervisory computer systems or data servers. The circuitry of the Control Processor is powered from the DC-DC converter, 246. The actions of the Control Processor are governed by embedded real-time executive and application-specific software to control the tasks, operation actions and methods described herein.

Please amend the paragraph on page 52, lines 15-31, as follows:

The Power Supply module 250 (Fig. 6[B]) contains circuitry to condition the mains input power supplied by line 254 and convert it from AC to DC for use by all of the system. This module comprises a manually or electrically controlled AC mains on/off control switch 252 with suitable protective fusing in the case of overload or short circuit faults and a transformer (or other means) 256 to produce AC power isolated from the mains for use in powering isolated AC motor and heater loads. Isolated AC power is distributed to every module of the system via line 212. In addition, the Power Supply 250 contains circuitry 260 to monitor the condition and quality of the AC mains supplied power, thus, indicating voltage reductions, drop-outs, surges and sags to the Control Processor 200 so that it can take corrective actions with respect to the operation of the system. Finally, this module contains circuitry to convert the AC input power to DC power at the various voltages and current levels needed by the system's other circuitry. This conversion is made by an auto-ranging input, low dissipation high-efficiency AC-DC converter 258 (or other means). The auto-ranging input stage of the AC-DC converter accommodates AC inputs from 90-275 VAC, 40-400 Hz. The output of this converter supplies regulated +24V DC to the Control Processor and all other subsystem modules via line 214.